PTO/SB/17 (10-07)
Approved for use through 06/30/2010. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Effective on 12/08/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2008

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT	($)	970.00

Complete if Known	
Application Number	10/511,640
Filing Date	October 18, 2004
First Named Inventor	Weixiao Liu et al.
Examiner Name	Kevin Michael Burd
Art Unit	2611
Attorney Docket No.	PU020138

METHOD OF PAYMENT (check all that apply)

☐ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☑ Deposit Account Deposit Account Number: 07-0832 Deposit Account Name: Thomson Licensing, LLC

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☑ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

☑ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17 ☑ Credit any overpayments

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
		Small Entity		Small Entity		Small Entity	
Application Type	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fees Paid ($)
Utility	310	155	510	255	210	105	
Design	210	105	100	50	130	65	
Plant	210	105	310	155	160	80	
Reissue	310	155	510	255	620	310	
Provisional	210	105	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	210	105
Multiple dependent claims	370	185

Total Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 20 or HP =	_____	x _____	= _____

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 3 or HP =	_____	x _____	= _____

HP = highest number of independent claims paid for, if greater than 3.

Multiple Dependent Claims	
Fee ($)	Fee Paid ($)
_____	_____

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $260 ($130 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee ($)	Fee Paid ($)
_____ - 100 =	_____	/ 50 = _____ (round up to a whole number)	x _____	= _____

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	
Other (e.g., late filing surcharge): Appeal Brief and Two (2) Month Extension of Time	$970.00

SUBMITTED BY

Signature		Registration No. (Attorney/Agent) 34,721	Telephone 212-971-0416
Name (Print/Type)	Jack Schwartz		Date February 27, 2008

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Before the Board of Patent Appeals and Interferences

Inventor:	Weixiao Liu et al.
Application No.:	10/511,640
Filed:	October 18, 2004
Title:	Symbol Timing Search Algorithm
Examiner:	Kevin Michael Burd
Art Unit:	2611

APPEAL BRIEF

May It Please The Honorable Board:

Appellants initiate a new appeal under 37 CFR 41.27 in response to the Final Rejection, dated July 31, 2007, of claims 1 - 15 of the above-identified application. The fee of five hundred ten dollars ($510.00) for filing this Brief and the fee of four hundred sixty dollars ($460.00) for extending the time for a response within the second month after the original response date, pursuant to 37 CFR 1.17(a)(2) is to be charged to Deposit Account No. 07-0832. Enclosed is a single copy of this Brief.

Please charge any additional fee or credit any overpayment to the above-identified Deposit Account.

03/03/2008 ATRINH 00000063 070832 10511640

01 FC:1402 510.00 DA
02 FC:1252 460.00 DA

Appellants do not request an oral hearing.

****

Certificate of Mailing under 37 CFR 1.8

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in a postage paid envelope addressed to: Mail Stop: Appeal Briefs - Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date indicated below.

Signature _____ Date: 2/27/08

I. REAL PARTY IN INTEREST

The real party in interest of Application Serial No. 10/511,640 is the Assignee of record:

Thomson Licensing S.A.

46 quai Alphonse Le Gallo

F-92100 Boulogne Billancourt

France

II. RELATED APPEALS AND INTERFERENCES

There are currently, and have been, no related Appeals or Interferences regarding Application Serial No. 10/511,640.

III. STATUS OF THE CLAIMS

Claims 1-15 are rejected and the rejection of claims 1-15 is appealed.

IV. STATUS OF AMENDMENTS

All amendments were entered and are reflected in the claims included in Appendix I.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 1 provides a method for establishing timing synchronism between a transmitter symbol clock (page 1, lines 24-25; page 2, lines 13-15; page 5, lines 21-22; figure 1, reference no. 60) and a local symbol clock in a receiver for receiving a signal transmitted as a sequence of symbols at a symbol frequency and subject to exhibiting a symbol frequency offset (page 2, lines 24-29; page 3, lines 22-26). A preselected number of offset values are calculated for a desired symbol timing recovery range (page 3, lines 15-17; page 3, lines 26-29; page 10, lines 16-20). The offset values are grouped substantially symmetrically about a central offset value (page 3, lines 26-29). Each of the preselected offset values is tested to see if symbol timing recovery lock can be achieved by starting at a central offset value (page 3, lines 18-20; page 9, lines 4-6; figure 2, reference no. 606) and gradually moving away from the central offset value (page 3, lines 18-20; page 3, line 29-page 4, line 2; page 9, lines 4-18).

Dependent claim 2 includes all the features of claim 1, along with the additional feature that the received signal carries a high definition television signal (HDTV) signal transmitted as a modulated vestigial sideband (VSB) signal formatted as a one-dimensional data constellation of symbols representing digital image data (page 4, lines 12-19).

Dependent claim 3 includes all the features of claim 1, along with the additional feature that the desired symbol timing recovery range is plus or minus 1 kHz (page 8, lines 22-23).

Dependent claim 4 includes all the features of claims 1 and 3, along with the additional feature that the preselected number of offset values is nine (page 8, lines 23-24).

Dependent claim 5 includes all the features of claims 1, 3 and 4, along with the additional feature that the nine offset values are 0 Hz, plus or minus 200 Hz, plus or minus 400 Hz, plus or minus 600 Hz and plus or minus 800 Hz (page 8, lines 23-24).

Dependent claim 6 includes all the features of claim 1, along with the additional steps of repeating the testing step for each of a plurality of symbol timing recovery algorithms (page 9, lines 17-18).

Dependent claim 7 includes all the features of claims 1 and 6, along with the additional feature that the plurality of symbol timing recovery algorithms include the Mueller and Muller algorithm and the Gardner algorithm (page 7, lines 22-25; page 8, lines 1-6; page 10, line 27-page 11, line 1).

Independent claim 8 provides a processor for establishing timing synchronism between a transmitter symbol clock (page 1, lines 24-25; page 2, lines 13-15; page 5, lines 21-22; figure 1, reference no. 60) and a local receiver symbol clock in a receiver for receiving a signal including a sequence of symbols at a symbol frequency and subject to exhibiting symbol frequency offset (page 2, lines 24-29; page 3, lines 22-26). A preselected number of offset values are calculated for a desired symbol timing recovery range (page 3, lines 15-17; page 3, lines 26-29; page 10, lines 16-20). The offset values are grouped substantially symmetrically about a central offset

value (page 3, lines 26-29). Each of the preselected offset values are tested to see if the symbol timing recovery lock can be achieved by starting at the central offset value (page 3, lines 18-20; page 9, lines 4-6; figure 2, reference no. 606) and gradually moving away from the central offset value (page 3, lines 18-20; page 3, line 29-page 4, line 2; page 9, lines 4-18).

Dependent claim 9 includes all the features of claim 8, along with the additional feature that the received signal includes a high definition television (HDTV) signal transmitted as a one-dimensional data constellation of symbols representing digital image data (page 4, lines 12-19).

Dependent claim 10 includes all the features of claim 8, along with the additional feature that the desired symbol timing recovery range is plus or minus 1 kHz (page 8, lines 22-23).

Dependent claim 11 includes all the features of claims 8 and 10, along with the additional feature that the preselected number of offset values is nine (page 8, lines 23-24).

Dependent claim 12 includes all the features of claims 8, 10 and 11 along with the additional feature that the nine offset values are 0 Hz, plus or minus 200 Hz, plus or minus 400 Hz, plus or minus 600 Hz and plus or minus 800 Hz (page 8, lines 23-24).

Dependent claim 13 includes all the features of claim 12, along with the additional feature of using a plurality of symbol timing detection algorithms for the testing and for switching between the algorithms as desired to maximize the possibility of STR lock (page 3, lines 20-21).

Dependent claim 14 includes all the features of claims 12 and 13, along with the additional feature of selecting one of the plurality of detection algorithms before testing each of the preselected offset values (page 3, liens 18-20).

Dependent claim 15 includes all the features of claims 8 and 13, along with the additional feature that the plurality of timing detection algorithms include the Mueller and Muller algorithm

and the Gardner algorithm (page 7, lines 22-25; page 8, lines 1-6; page 10, line 27-page 11, line 1).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Figure 1 of the Drawings is objected to as being the same as figure 1 of Wang (U.S. Patent No. 6,266,380).

Claims 1, 3-6, 8 and 10-13 are rejected under 35 U.S.C. § 102(b) as being anticipated by Shanley, II (U.S. Patent No. 4,617,587), hereinafter "Shanley."

Claims 2 and 9 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Shanley, II (U.S. Patent No. 4,617,587) in view of Wang (U.S. Patent No. 6,266,380).

Claims 7 and 15 are rejected under 35 U.S.C. § 103(a) as being unpatentable Shanley, II (U.S. Patent No. 4,617,587) in view of Guillemain et al. (U.S. Patent No. 6175,600), hereinafter "Guillemain."

VII. ARGUMENT

Figure 1 of the Drawings of the present invention describes a different invention than figure 1 of Wang (U.S. Patent No. 6,266,380).

Objection to the Drawings

Figure 1 has been objected to for omitting the legend "—Prior Art—." However, Applicants respectfully submit that while Figure 1 of the present claimed invention and Fig. 1 of Wang (U.S. Patent No. 6,266,380) may contain similar block diagram headings, the functions performed by the present claimed invention as well as the elements depicted in Figure 1 are different than the functions performed by Wang. More specifically, the present claimed invention in Figure 1 contains a block identified by reference numeral 60 and the legend

"SEGMENT SYNC AND SYMBOL CLK. RECOVERY." Fig. 1 of Wang includes a block identified with the reference numeral 24 and a similar legend. However, the two similarly titled blocks perform different methods of segmenting the synchronization and symbol clock recovery. In the present claimed invention, "the STR symbol frequency offset in the circuit 60 is set during the acquisition phase to different values chosen from the range of offsets that the STR is likely to traverse. In a preferred embodiment of the present invention the STR offset range is specified to be ± 1 kHz. This range is partitioned into nine points which corresponds to offsets of 0, ± 200 Hz, ± 400 Hz, ± 600 Hz, and ± 800 Hz from the nominal symbol frequency" (Specification, page 8, lines 19-24). Contrary to the present claimed invention, block 24 in Fig. 1 of Wang "detects and separates the repetitive data segment sync components of each data frame from the random data" (col. 2, lines 57-58). Wang does not specify the STR offset range to be partitioned into nine points as in the present claimed invention. Therefore, the functions performed in Figure 1 of the present claimed invention are different from the functions performed in Fig. 1 of Wang. This difference is also emphasized in the specification and claims of the present invention.

Additionally, the "Response to Arguments" section, of the Office Action contends that the receiver shown in Figure 1 of the present claimed invention is the same as the figure in Wang. Applicants respectfully disagree. Although the figures appear similar, the functions performed by the components as described in the Specification of the present claimed invention are completely different than the functions performed by the components in the figure in Wang. Specifically, the STR symbol frequency offset range in Figure 1, block 60 of the present claimed invention is preferably set to be ± 1 kHz and is partioned into nine points. This is neither disclosed nor suggested by Wang. Wang, contrary to the present claimed invention, does not disclose or suggest a segment synchronization and symbol clock recovery capable of performing the functions described in the present claimed invention. Therefore, Figure 1 of the present claimed invention as described in the Specification does not illustrate a prior art system and Applicants respectfully submit it would not be proper to identify the figure as such.

MPEP 2129, section II, describes that "[w]here the specification identifies work done by another as 'prior art,' the subject matter so identified is treated as admitted prior art." As discussed in the Specification, the functions of the elements shown in Figure 1 of the present

claimed invention are clearly different than the functions of the elements shown in Fig. 1 of Wang. Applicants respectfully submit that Figure 1 of the present application is not prior art, and furthermore, the present claims in view of Figure 1 (and Figure 2) and the Specification are not anticipated by Wang. More specifically, the Specification does NOT admit that Figure 1 is "prior art" but rather describes the inventive features of the present claimed invention (*see* Specification, page 4, line 11-page 8, line 28). Furthermore, Wang is incapable of performing the features shown in Figure 1, block 60 of the present claimed invention because Wang is not concerned with and does not show the feature of "establishing timing synchronism between a transmitter symbol clock and a local symbol clock in a receiver ... calculating a preselected number of offset values for a desired symbol timing recovery range, said offset values being grouped substantially symmetrically about a central offset value; testing each of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value" as recited in claim 1 of the present invention. As shown in Figure 1, block 60 of the present claimed invention, the "Segment Sync and Symbol Clock Recovery" apparatus is incorporated to perform the step of "establishing timing synchronism between a transmitter symbol clock and a local symbol clock in a receiver" as recited in claim 1 of the present invention. Moreover, Applicants further respectfully submit that Fig. 1 of Wang is NOT considered prior art because the Office Action does not cite Wang as anticipating the present claimed invention under 35 U.S.C. 102. Therefore, as the present claimed invention is not anticipated by Wang, Figure 1 is not prior art in view of Fig. 1 of Wang.

Additionally, MPEP § 608.02(e) recites that "[t]he examiner should see to it that the figures are correctly described in the brief description of the ... drawing section of the specification." As the "Brief Description of the Drawings" section of the Specification provides that "Fig. 1 is a block diagram of a VSB receiver incorporating the **principles of the present invention**," Applicants respectfully submit that Figure 1 shows the features of present claimed invention (in view of the Specification) and is not prior art in view of Wang. Therefore, Figure 1 of the present claimed invention performs different functions than Fig. 1 of Wang, and Wang does not anticipate the present claimed invention under 35 U.S.C. 102. In view of the above

remarks regarding Figure 1 it is respectfully submitted that this objection is satisfied and should be withdrawn.

Shanley does not anticipate claims 1, 3-6, 8 and 10-13. Thus, reversal of the rejection of claims 1, 3-6, 8 and 10-13 under 35 U.S.C. § 102(b) is respectfully requested. Additionally, Shanley in view of Wang does not make claims 2 and 9 unpatentable. Thus, reversal of the rejection of claims 2 and 9 under 35 U.S.C. § 103(a) is respectfully requested. Moreover, Shanley in view of Guillemain does not make claims 7 and 15 unpatentable. Thus, reversal of the rejection of claims 7 and 15 under 35 U.S.C. § 103(a) is respectfully requested. Reversal of the Final Rejection (hereinafter termed "rejection") of claims 1-15 under 35 U.S.C. § 102(b) and 35 U.S.C. § 103(a) is respectfully requested and reversal of the objection to the Drawings is respectfully requested.

Overview of the Cited References

Shanley describes a non-inverting amplifier, with a bandpass filter in a regenerative feedback path that forms color reference oscillator in a color TV receiver. A phase shift circuit, responsive to an oscillator output, supplies signals to a first phase shifted signal amplifier, which shares a load with the non-inverting amplifier, and is subject to control by complementary outputs of a phase comparator functioning to compare the phase of an oscillator output with the phase of incoming color synchronizing bursts. A voltage comparator, responsive to the respective phase comparator outputs, is periodically enabled by field rate keying pulses. The voltage comparator output controls the charging or discharging of a capacitor during the keying intervals. A second phase shifted signal amplifier, responsive to the output of the phase shift circuit, and delivering its output to the oscillator's feedback path, is subject to control in dependence upon a comparison of a control voltage derived from the voltage held by the capacitor with a reference DC voltage. A latching circuit, subject to disabling only when receiver's color killer circuit operates in a color unkilling mode, is switched into a first latched mode of operation if voltage held by capacitor reaches a first extreme of its variation range, the first latched mode of operation forcing an unbalance of a first sense upon the voltage comparator inputs. The latching circuit is switched into a second latched mode of operation, forcing an

opposite sense unbalance upon the voltage comparator inputs, if voltage held by capacitor reaches opposite extreme of its variation range (*see* Abstract).

Wang describes a receiver for processing a VSB modulated signal containing terrestrial broadcast high definition television information and a pilot component includes an input analog-to-digital converter (19) for producing a datastream which is oversampled at twice the received symbol rate, and a digital demodulator with a data reduction network in a phase control loop. A segment sync detector uses an abbreviated correlation reference pattern to recover a twice symbol rate sampling clock for the digital converter. A DC offset associated with the pilot component is removed from the demodulated signal before it is applied to an NTSC interference detection network. The interference detection network includes a comb filter network dimensioned to avoid aliasing in the combed frequency spectrum, thereby increasing the effectiveness of NTSC co-channel interference detection (*see* Abstract).

Guillemain describes a system for detecting the presence of a carrier wave in a digital signal that is available at a given frequency. The system delivers at least two baseband samples of the digital signal at each symbol time. The system comprises a timing estimator responsive to the baseband samples to deliver an error signal corresponding to the phase error between the clock frequency that is to be recovered and a local clock frequency, and a detector that generates a detection signal indicating that a carrier wave has been detected whenever a level representative of the variance of the error signal reaches a threshold value. The invention is particularly applicable to receivers of signals transmitted in DTMA mode (*see* Abstract).

Rejection of claims 1, 3-6, 8 and 10-13 under 35 U.S.C. 102(b) over Shanley, II (U.S. Patent No. 4,617,587)

Reversal of the rejection of claims 1, 3-6, 8 and 10-13 under 35 U.S.C. § 102(b) as being anticipated by Shanley, II (U.S. Patent No. 4,617,587) is respectfully requested because the rejection makes crucial errors in interpreting the cited reference. The rejection erroneously states that claims 1, 3-6, 8 and 10-13 are anticipated by Shanley.

CLAIM 1

Independent claim 1 provides a method for establishing timing synchronism between a transmitter symbol clock and a local symbol clock in a receiver for receiving a signal transmitted as a sequence of symbols at a symbol frequency and subject to exhibiting a symbol frequency offset. A preselected number of offset values are calculated for a desired symbol timing recovery range. The offset values are grouped substantially symmetrically about a central offset value. Each of the preselected offset values is tested to see if symbol timing recovery lock can be achieved by starting at a central offset value and gradually moving away from the central offset value. Shanley neither discloses nor suggests these features of the present claimed invention.

More specifically, Shanley neither discloses nor suggests "calculating a preselected number of offset values for a desired symbol timing recovery range, said offset values being grouped substantially symmetrically about a central offset value" as recited in claim 1 of the present invention. Additionally, Shanley neither discloses nor suggests "testing each of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value" as recited in claim 1 of the present invention.

Shanley "relates generally to control loops for use in automatically establishing a desired condition of operation of electrical apparatus, and particularly to a recovery system for use with such a control loop to enable recovery from a failure mode in which a control voltage may be spuriously driven to a control voltage range extreme without establishing the desired operating condition" (col. 1, lines 5-11).

Shanley describes "a control loop employed to effect color synchronization in a color television receiver" (col. 1, lines 12-14). "The phase comparator and the phase shifted signal amplifier cooperate with the local color oscillator to form a phase locked loop, the loop functioning to lock the oscillator frequency and phase to the incoming color synchronizing bursts. When the free-running frequency of the oscillator is equal to the subcarrier frequency of

the incoming synchronizing bursts ... accurate phasing of reference oscillations ... is readily attainable. However, when the phase locked loop achieves locking in instances where the free-running frequency of the local oscillator is not equal to the subcarrier frequency of the incoming bursts, the loop will have stabilized in a condition appropriate to achievement of an alteration of the oscillator frequency " (col. 2, lines 18-37). When this occurs, a static phase error occurs (see col. 2, lines 39-54) and the oscillator frequency is adjusted (see col. 12, lines 16-24) for synchronization. Thus, Shanley merely synchronizes the free-running frequency of the local oscillator with the subcarrier frequency of the incoming bursts in order to properly display colors in NTSC or PAL type television receivers (see col. 2, lines 47-54). However, Shanley neither discloses nor suggests "calculating **a preselected number of offset values** for a desired symbol timing recovery range, said offset values being grouped substantially symmetrically about a central offset value" as recited in claim 1 of the present invention. Furthermore, as Shanley does not calculate a preselected number of offset values, Shanley also neither discloses nor suggests "testing each of the preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value" as recited in claim 1 of the present invention.

The Office Action cites col. 12, lines 52-64 of Shanley as being equivalent to the present claimed invention. Applicants respectfully disagree. This passage of Shanley recites:

> "the recovery apparatus effectively functions to 'sweep' the oscillator's free-running frequency in discrete steps from a remote range edge frequency in a direction lessening the difference between the oscillator frequency and the subcarrier frequency. This sweep capability permits recovery from the consequences of a 'wrong-direction' start; the subsequent 'right-direction' sweep continues until the shifted pull-in range of the oscillator encompasses the subcarrier frequency, allowing lock to be attained by the phase locked loop (31, 32) during the burst comparisons of the succeeding field interval" (Col. 12, lines 53-64).

Nowhere in the above cited passage or anywhere else in Shanley is there mention or suggestion of "calculating a preselected number of offset values for a desired symbol timing recovery range" as recited in the present claimed invention. Furthermore, contrary to the assertions made in the Office Action, the "sweeps" performed in Shanley are not performed at a central offset value, as Shanley does not calculate any "offset values" and therefore, cannot group the offset values "substantially symmetrically about a central offset value" as recited in the present claimed

invention. Additionally, as "a preselected number of offset values for a desired symbol timing recovery range" are not calculated by Shanley, Shanley also cannot test "each of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value" as recited in the present claimed invention. Therefore, Shanley does not disclose or suggest the features of the present claimed invention.

Additionally, in the "Response to Arguments" section of the Office Action, it is contended that Shanley discloses all the features of the present invention. Specially, the Office Action asserts that "Shanley states 'the recovery apparatus effectively functions to 'sweep' the oscillator's free running frequency in discrete steps from a remote range edge frequency in a direction lessening the difference between oscillator frequency and subcarrier frequency' in column 12, lines 52-64. Each of the discrete steps is a frequency offset value and each offset will be tested to see if a lock has occurred between the oscillator frequency and the subcarrier frequency. The discrete steps are the frequency offset values since the steps are the difference between the present frequency and the starting frequency. The sweeping of the frequency in these discrete steps (offsets) will continue until a frequency lock occurs (column 12, lines 52-64). Therefore, the receiver always determines if the present frequency is locked with the subcarrier frequency." Applicants respectfully submit that nowhere in the cited passage or elsewhere in Shanley is there mention or suggestion of "**calculating** a preselected number of offset values for a desired symbol timing recovery range, said offset values being grouped substantially symmetrically about a central offset value; testing each of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value" as recited in claim 1 of the present invention. The present claimed invention recognizes that "it may take a long time for the symbol timing recovery circuit to acquire a 'lock' on a channel if the starting point of the symbol timing recovery (STR) loop integrator (e.g. the loop integrator output signal for the previous signal) is far away from the eventual locked value for the new signal ... Indeed, if the STR starting offset is too far away from the locked value, STR loop lock may not be reliably achieved at all" (Specification, page 3, lines 2-8). The present claimed invention therefore is able to maximize the possibility of STR lock by grouping a calculated "preselected number of offset values for a

desired symbol timing recover range ... substantially symmetrically about a central offset value" as recited in claim 1 of the present invention. Additionally, the present claimed invention "quickly and reliably establish[es] timing synchronism between the receiver symbol clock and the transmitter symbol clock" (Specification, page 8, lines 25-26). Shanley is not concerned with and does not disclose or suggest "calculating a preselected number of offset values for a desired symbol timing recovery range, said offset values being grouped substantially symmetrically about a central offset value" as recited in claim 1 of the present invention, but rather only attains lock loop by performing a sweep of the oscillator's free running frequency in discrete steps. Furthermore, as described above, the cited passage of Shanley describes that "the recovery apparatus effectively functions to 'sweep' the oscillator's free-running frequency in discrete steps from a remote range edge frequency in a direction lessening the difference between oscillator and subcarrier frequency ... sweep continues until the shifted pull-in range of the oscillator encompasses the subcarrier frequency allowing lock to be attained by the phase locked loop" (col. 12, lines 53-62). However, merely sweeping the oscillator's free-running frequency (in discrete steps) from a remote range edge frequency in a direction lessening the difference between the oscillator frequency and the subcarrier frequency, as in Shanley, is not the same as having a **calculated preselected** number of offset values, where the "offset values ... [are] grouped substantially symmetrically about a central offset value" as recited in claim 1 of the present invention. Rather, Shanley may sweep all or any frequencies, until a lock is attained. This is wholly unlike the present claimed invention, which is concerned with "calculating a preselected number of offset values for a desired symbol timing recovery range, said offset values being grouped substantially symmetrically about a central offset value." Moreover, as preselected offset values are NOT calculated by Shanley, Shanley cannot disclose or suggest the "testing [of] each of said **preselected offset values** to see if symbol timing recovery lock can be achieved by starting at said **central offset value** and gradually moving away from said central offset value" as recited in claim 1 of the present invention.

Therefore as Shanley fails to show or suggest each feature in claim 1, Shanley does not anticipate the present claimed invention. Consequently, it is respectfully requested that the rejection of claim 1 under 35 U.S.C. 102(b) be withdrawn.

CLAIM 3

Claim 3 is dependent on claim 1 and is considered patentable for the reasons discussed above with respect to claim 1. Claim 3 is also considered patentable because Shanley fails to disclose or suggest that the "desired symbol timing recovery range is plus or minus 1 kHz" as recited in claim 3 of the present invention. In the present claimed invention, "the STR offset range is specified to be ± 1 kHz" (Specification, page 8, lines 22-23). Nowhere in Shanley is there suggestion or disclosure that the "desired symbol timing recovery range is plus or minus 1 kHz" as recited in claim 3 of the present invention. Rather, Shanley is merely concerned with "allowing lock to be attained by the phase locked loop (31, 32) during the burst comparisons of the succeeding filed interval" (col. 12, lines 62-64). To the contrary, the present claimed invention specifically defines an STR offset range in order to first calculate a preselected number of offset values for the desired symbol timing recovery range and then test "each of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value" as recited in the present claimed invention. Therefore, Shanley neither discloses nor suggests that the "desired symbol timing recovery range is plus or minus 1 kHz" as recited in claim 3 of the present invention.

Therefore as Shanley fails to show or suggest each feature in claim 3, Shanley does not anticipate the present claimed invention. Consequently, it is respectfully requested that the rejection of claim 3 under 35 U.S.C. 102(b) be withdrawn.

CLAIM 4

Claim 4 is dependent on claims 1 and 3 and is considered patentable for the reasons discussed above with respect to claims 1 and 3. Claim 4 is also considered patentable because Shanley fails to disclose or suggest that the "preselected number of offset values is nine" as recited in claim 4 of the present invention. In the present claimed invention, "the STR offset range is specified to be ± 1 kHz. This range is partitioned into nine points which corresponds to offsets of 0, ± 200 Hz, ± 400 Hz, ± 600 Hz, and ± 800 Hz from the nominal symbol frequency" (Specification, page 8, lines 22-24). Nowhere in Shanley is there suggestion or disclosure that the "preselected number of offset values is nine" as recited in claim 4 of the present invention.

Rather, Shanley is merely concerned with "allowing lock to be attained by the phase locked loop (31, 32) during the burst comparisons of the succeeding filed interval" (col. 12, lines 62-64). Shanley does not specifically disclose or suggest that the preselected number of offset values is nine. Shanley is not concerned with and does not show the feature of having nine preselected offset values, as in the present claimed invention, because Shanley only obtains phase locked loop by sweeping. The "sweep capability permits recovery from the consequences of a 'wrong-direction' start; the subsequent 'right-direction' sweep continues until the shifted pull-in range of the oscillator encompasses the subcarrier frequency, allowing lock to be attained" (col. 12, lines 57-62). To the contrary, the present claimed invention specifically defines an STR offset range which is partitioned into nine values in order to test "each of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value" as recited in the present claimed invention.

Additionally, the Office Action on page 5 contends that "Shanley discloses the sweep will be conducted in discrete steps and continue until the lock is attained. The number of steps can be any number that allows this to occur including nine." Applicants respectfully disagree. Although Shanley is concerned with attaining a lock, Shanley fails to specifically disclose that the "**preselected** number of offset values is nine," as recited in claim 4 of the present invention. Therefore, Shanley neither discloses nor suggests that the "preselected number of offset values is nine" as recited in claim 4 of the present invention.

Therefore as Shanley fails to show or suggest each feature in claim 4, Shanley does not anticipate the present claimed invention. Consequently, it is respectfully requested that the rejection of claim 4 under 35 U.S.C. 102(b) be withdrawn.

CLAIM 5

Claim 5 is dependent on claims 1, 3 and 4 and is considered patentable for the reasons discussed above with respect to claims 1, 3 and 4. Claim 5 is also considered patentable because Shanley fails to disclose or suggest that the "nine offset values are 0 Hz; plus or minus 200 Hz; plus or minus 400 Hz; plus or minus 600 Hz; and plus or minus 800 Hz" as recited in claim 5 of

the present invention. In the present claimed invention, "the STR offset range is specified to be ± 1 kHz. This range is partitioned into nine points which corresponds to offsets of 0, ± 200 Hz, ± 400 Hz, ± 600 Hz, and ± 800 Hz from the nominal symbol frequency" (Specification, page 8, lines 22-24). Nowhere in Shanley is there suggestion or disclosure that the "nine offset values are 0 Hz; plus or minus 200 Hz; plus or minus 400 Hz; plus or minus 600 Hz; and plus or minus 800 Hz" as recited in claim 5 of the present invention. Rather, Shanley is merely concerned with "allowing lock to be attained by the phase locked loop (31, 32) during the burst comparisons of the succeeding filed interval" (col. 12, lines 62-64). Shanley does not specifically disclose or suggest that the nine offset values are 0, ± 200 Hz, ± 400 Hz, ± 600 Hz, and ± 800 Hz. In fact, Shanley is not even concerned with and does not show the feature of having nine preselected offset values let alone offset values of 0, ± 200 Hz, ± 400 Hz, ± 600 Hz, and ± 800 Hz, as in the present claimed invention, because Shanley only obtains phase locked loop by sweeping. The "sweep capability permits recovery from the consequences of a 'wrong-direction' start; the subsequent 'right-direction' sweep continues until the shifted pull-in range of the oscillator encompasses the subcarrier frequency, allowing lock to be attained" (col. 12, lines 57-62). To the contrary, the present claimed invention specifically defines an STR offset range which is partitioned into nine values in order to test "each of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value" as recited in the present claimed invention.

Additionally, the Office Action on page 5 contends that "Shanley discloses the sweep will be conducted in discrete steps and continue until the lock is attained. The number of steps can be any number that allows this to occur including nine and the discrete steps can be any discrete value that allows the lock to take place including 200 Hz." Applicants respectfully disagree. Although Shanley is concerned with attaining a lock, Shanley fails to specifically disclose that the "nine offset values are 0 Hz; plus or minus 200 Hz; plus or minus 400 Hz; plus or minus 600 Hz; and plus or minus 800 Hz," as recited in claim 5 of the present invention. Therefore, as there is no mention or suggestion in Shanley of the nine offset values in claim 5, Shanley neither discloses nor suggests that the "nine offset values are 0 Hz; plus or minus 200

Hz; plus or minus 400 Hz; plus or minus 600 Hz; and plus or minus 800 Hz" as recited in claim 5 of the present invention.

Therefore as Shanley fails to show or suggest each feature in claim 5, Shanley does not anticipate the present claimed invention. Consequently, it is respectfully requested that the rejection of claim 5 under 35 U.S.C. 102(b) be withdrawn.

CLAIM 6

Claim 6 is dependent on claim 1 and is considered patentable for the reasons discussed above with respect to claim 1. Claim 6 is also considered patentable because Shanley fails to disclose or suggest "**repeating** the testing step for each of a plurality of symbol timing recovery algorithms" as recited in claim 6 of the present invention. Rather, Shanley is merely concerned with "allowing lock to be attained by the phase locked loop (31, 32) during the burst comparisons of the succeeding filed interval" (col. 12, lines 62-64). Shanley does not specifically disclose or suggest "testing each of said preselected offset values" and therefore cannot repeat the testing step. Therefore, Shanley neither discloses nor suggests "repeating the testing step for each of a plurality of symbol timing recovery algorithms" as recited in claim 6 of the present invention.

Therefore as Shanley fails to show or suggest each feature in claim 6, Shanley does not anticipate the present claimed invention. Consequently, it is respectfully requested that the rejection of claim 6 under 35 U.S.C. 102(b) be withdrawn.

CLAIM 8

Independent claim 8 provides a processor for establishing timing synchronism between a transmitter symbol clock and a local receiver symbol clock in a receiver for receiving a signal including a sequence of symbols at a symbol frequency and subject to exhibiting symbol frequency offset. A preselected number of offset values are calculated for a desired symbol timing recovery range. The offset values are grouped substantially symmetrically about a central offset value. Each of the preselected offset values are tested to see if the symbol timing recovery lock can be achieved by starting at the central offset value and gradually moving away from the

central offset value. Shanley neither discloses nor suggests these features of the present claimed invention.

Shanley neither discloses nor suggests "means for calculating a preselected number of offset values for a desired symbol timing recovery range, said offset values being grouped substantially symmetrically about a central offset value" as recited in claim 8 of the present invention. Additionally, Shanley neither discloses nor suggests "means for testing each of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value" as recited in claim 8 of the present invention.

Shanley "relates generally to control loops for use in automatically establishing a desired condition of operation of electrical apparatus, and particularly to a recovery system for use with such a control loop to enable recovery from a failure mode in which a control voltage may be spuriously driven to a control voltage range extreme without establishing the desired operating condition" (col. 1, lines 5-11).

Shanley describes "a control loop employed to effect color synchronization in a color television receiver" (col. 1, lines 12-14). "The phase comparator and the phase shifted signal amplifier cooperate with the local color oscillator to form a phase locked loop, the loop functioning to lock the oscillator frequency and phase to the incoming color synchronizing bursts. When the free-running frequency of the oscillator is equal to the subcarrier frequency of the incoming synchronizing bursts ... accurate phasing of reference oscillations ... is readily attainable. However, when the phase locked loop achieves locking in instances where the free-running frequency of the local oscillator is not equal to the subcarrier frequency of the incoming bursts, the loop will have stabilized in a condition appropriate to achievement of an alteration of the oscillator frequency " (col. 2, lines 18-37). When this occurs, a static phase error occurs (see col. 2, lines 39-54) and the oscillator frequency is adjusted (see col. 12, lines 16-24) for synchronization. Thus, Shanley merely synchronizes the free-running frequency of the local oscillator with the subcarrier frequency of the incoming bursts in order to properly display colors in NTSC or PAL type television receivers (see col. 2, lines 47-54). However, Shanley neither

discloses nor suggests "means for **calculating a preselected number of offset values** for a desired symbol timing recovery range, said offset values being grouped substantially symmetrically about a central offset value" as recited in claim 8 of the present invention. Furthermore, as Shanley does not calculate a preselected number of offset values, Shanley also neither discloses nor suggests "means for testing each of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value" as recited in claim 8 of the present invention.

The Office Action cites col. 12, lines 52-64 of Shanley as being equivalent to the present claimed invention. Applicants respectfully disagree. In the cited passage, Shanley describes that

> "the recovery apparatus effectively functions to 'sweep' the oscillator's free-running frequency in discrete steps from a remote range edge frequency in a direction lessening the difference between the oscillator frequency and the subcarrier frequency. This sweep capability permits recovery from the consequences of a 'wrong-direction' start; the subsequent 'right-direction' sweep continues until the shifted pull-in range of the oscillator encompasses the subcarrier frequency, allowing lock to be attained by the phase locked loop (31, 32) during the burst comparisons of the succeeding field interval" (Col. 12, lines 53-64).

Nowhere in the above cited passage or anywhere else in Shanley is there mention or suggestion of "calculating a preselected number of offset values for a desired symbol timing recovery range" as recited in the present claimed invention. Furthermore, contrary to the assertions made in the Office Action, the "sweeps" performed in Shanley are not performed at a central offset value, as Shanley does not calculate any "offset values" and therefore, cannot group the offset values "substantially symmetrically about a central offset value" as recited in the present claimed invention. Additionally, as "a preselected number of offset values for a desired symbol timing recovery range" are not calculated by Shanley, Shanley also cannot test "each of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value" as recited in the present claimed invention. Therefore, Shanley does not disclose or suggest the features of the present claimed invention.

Additionally, in the "Response to Arguments" section of the Office Action, it is

contended that Shanley discloses all the features of the present invention. Specially, the Office Action asserts that "Shanley states 'the recovery apparatus effectively functions to 'sweep' the oscillator's free running frequency in discrete steps from a remote range edge frequency in a direction lessening the difference between oscillator frequency and subcarrier frequency' in column 12, lines 52-64. Each of the discrete steps is a frequency offset value and each offset will be tested to see if a lock has occurred between the oscillator frequency and the subcarrier frequency. The discrete steps are the frequency offset values since the steps are the difference between the present frequency and the starting frequency. The sweeping of the frequency in these discrete steps (offsets) will continue until a frequency lock occurs (column 12, lines 52-64). Therefore, the receiver always determines if the present frequency is locked with the subcarrier frequency." Applicants respectfully submit that nowhere in the cited passage or elsewhere in Shanley is there mention or suggestion of "means for calculating a preselected number of offset values for a desired symbol timing recovery range, said offset values being grouped substantially symmetrically about a central offset value; means for testing each of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value" as recited in claim 8 of the present invention. The present claimed invention recognizes that "it may take a long time for the symbol timing recovery circuit to acquire a 'lock' on a channel if the starting point of the symbol timing recovery (STR) loop integrator (e.g. the loop integrator output signal for the previous signal) is far away from the eventual locked value for the new signal ... Indeed, if the STR starting offset is too far away from the locked value, STR loop lock may not be reliably achieved at all" (Specification, page 3, lines 2-8). The present claimed invention therefore is able to maximize the possibility of STR lock by grouping a calculated "preselected number of offset values for a desired symbol timing recover range ... substantially symmetrically about a central offset value" as recited in claim 8 of the present invention. Additionally, the present claimed invention "quickly and reliably establish[es] timing synchronism between the receiver symbol clock and the transmitter symbol clock" (Specification, page 8, lines 25-26). Shanley is not concerned with and does not disclose or suggest "calculating a preselected number of offset values for a desired symbol timing recovery range, said offset values being grouped substantially symmetrically about a central offset value" as recited in claim 8 of the present invention, but rather only attains lock loop by performing a sweep of the oscillator's free running frequency in

discrete steps. Furthermore, as described above, the cited passage of Shanley describes that "the recovery apparatus effectively functions to 'sweep' the oscillator's free-running frequency in discrete steps from a remote range edge frequency in a direction lessening the difference between oscillator and subcarrier frequency ... sweep continues until the shifted pull-in range of the oscillator encompasses the subcarrier frequency allowing lock to be attained by the phase locked loop" (col. 12, lines 53-62). However, merely sweeping the oscillator's free-running frequency (in discrete steps) from a remote range edge frequency in a direction lessening the difference between the oscillator frequency and the subcarrier frequency, as in Shanley, is not the same as having a **calculated preselected** number of offset values, where the "offset values ... [are] grouped substantially symmetrically about a central offset value" as recited in claim 8 of the present invention. Rather, Shanley may sweep all or any frequencies, until a lock is attained. This is wholly unlike the present claimed invention, which is concerned with "calculating a preselected number of offset values for a desired symbol timing recovery range, said offset values being grouped substantially symmetrically about a central offset value." Moreover, as preselected offset values are NOT calculated by Shanley, Shanley cannot disclose or suggest "means for testing each of said **preselected offset values** to see if symbol timing recovery lock can be achieved by starting at said **central offset value** and gradually moving away from said central offset value" as recited in claim 8 of the present invention.

Therefore as Shanley fails to show or suggest each feature in claim 8, Shanley does not anticipate the present claimed invention. Consequently, it is respectfully requested that the rejection of claim 8 under 35 U.S.C. 102(b) be withdrawn.

CLAIM 10

Claim 10 is dependent on claim 8 and is considered patentable for the reasons discussed above with respect to claim 8. Claim 10 is also considered patentable because Shanley fails to disclose or suggest that the "desired symbol timing recovery range is plus or minus 1 kHz" as recited in claim 10 of the present invention. In the present claimed invention, "the STR offset range is specified to be ± 1 kHz" (Specification, page 8, lines 22-23). Nowhere in Shanley is there suggestion or disclosure that the "desired symbol timing recovery range is plus or minus 1 kHz" as recited in claim 10 of the present invention. Rather, Shanley is merely concerned with

"allowing lock to be attained by the phase locked loop (31, 32) during the burst comparisons of the succeeding filed interval" (col. 12, lines 62-64). To the contrary, the present claimed invention specifically defines an STR offset range in order to first calculate a preselected number of offset values for the desired symbol timing recovery range and then test "each of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value" as recited in the present claimed invention. Therefore, Shanley neither discloses nor suggests that the "desired symbol timing recovery range is plus or minus 1 kHz" as recited in claim 10 of the present invention.

Therefore as Shanley fails to show or suggest each feature in claim 10, Shanley does not anticipate the present claimed invention. Consequently, it is respectfully requested that the rejection of claim 10 under 35 U.S.C. 102(b) be withdrawn.

CLAIM 11

Claim 11 is dependent on claims 8 and 10 and is considered patentable for the reasons discussed above with respect to claims 8 and 10. Claim 11 is also considered patentable because Shanley fails to disclose or suggest that the "preselected number of offset values is nine" as recited in claim 11 of the present invention. In the present claimed invention, "the STR offset range is specified to be ± 1 kHz. This range is partitioned into nine points which corresponds to offsets of 0, ± 200 Hz, ± 400 Hz, ± 600 Hz, and ± 800 Hz from the nominal symbol frequency" (Specification, page 8, lines 22-24). Nowhere in Shanley is there suggestion or disclosure that the "preselected number of offset values is nine" as recited in claim 11 of the present invention. Rather, Shanley is merely concerned with "allowing lock to be attained by the phase locked loop (31, 32) during the burst comparisons of the succeeding filed interval" (col. 12, lines 62-64). Shanley does not specifically disclose or suggest that the preselected number of offset values is nine. Shanley is not concerned with and does not show the feature of having nine preselected offset values, as in the present claimed invention, because Shanley only obtains phase locked loop by sweeping. The "sweep capability permits recovery from the consequences of a 'wrong-direction' start; the subsequent 'right-direction' sweep continues until the shifted pull-in range of the oscillator encompasses the subcarrier frequency, allowing lock to be attained" (col. 12, lines

57-62). To the contrary, the present claimed invention specifically defines an STR offset range which is partitioned into nine values in order to test "each of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value" as recited in the present claimed invention.

Additionally, the Office Action on page 5 contends that "Shanley discloses the sweep will be conducted in discrete steps and continue until the lock is attained. The number of steps can be any number that allows this to occur including nine." Applicants respectfully disagree. Although Shanley is concerned with attaining a lock, Shanley fails to specifically disclose that the "**preselected** number of offset values is nine," as recited in claim 11 of the present invention. Therefore, Shanley neither discloses nor suggests that the "preselected number of offset values is nine" as recited in claim 11 of the present invention.

Therefore as Shanley fails to show or suggest each feature in claim 11, Shanley does not anticipate the present claimed invention. Consequently, it is respectfully requested that the rejection of claim 11 under 35 U.S.C. 102(b) be withdrawn.

CLAIMS 12 and 13

Claim 12 is dependent on claims 8, 10 and 11 and is considered patentable for the reasons discussed above with respect to claims 8, 10 and 11. Claim 12 is also considered patentable because Shanley fails to disclose or suggest that the "nine offset values are 0 Hz; plus or minus 200 Hz; plus or minus 400 Hz; plus or minus 600 Hz; and plus or minus 800 Hz" as recited in claim 12 of the present invention. In the present claimed invention, "the STR offset range is specified to be ± 1 kHz. This range is partitioned into nine points which corresponds to offsets of 0, ± 200 Hz, ± 400 Hz, ± 600 Hz, and ± 800 Hz from the nominal symbol frequency" (Specification, page 8, lines 22-24). Nowhere in Shanley is there suggestion or disclosure that the "nine offset values are 0 Hz; plus or minus 200 Hz; plus or minus 400 Hz; plus or minus 600 Hz; and plus or minus 800 Hz" as recited in claim 12 of the present invention. Rather, Shanley is merely concerned with "allowing lock to be attained by the phase locked loop (31, 32) during the burst comparisons of the succeeding filed interval" (col. 12, lines 62-64). Shanley does not

specifically disclose or suggest that the nine offset values are 0, ± 200 Hz, ± 400 Hz, ± 600 Hz, and ± 800 Hz. In fact, Shanley is not even concerned with and does not show the feature of having nine preselected offset values let alone offset values of 0, ± 200 Hz, ± 400 Hz, ± 600 Hz, and ± 800 Hz, as in the present claimed invention, because Shanley only obtains phase locked loop by sweeping. The "sweep capability permits recovery from the consequences of a 'wrong-direction' start; the subsequent 'right-direction' sweep continues until the shifted pull-in range of the oscillator encompasses the subcarrier frequency, allowing lock to be attained" (col. 12, lines 57-62). To the contrary, the present claimed invention specifically defines an STR offset range which is partitioned into nine values in order to test "each of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value" as recited in the present claimed invention.

Additionally, the Office Action on page 5 contends that "Shanley discloses the sweep will be conducted in discrete steps and continue until the lock is attained. The number of steps can be any number that allows this to occur including nine and the discrete steps can be any discrete value that allows the lock to take place including 200 Hz." Applicants respectfully disagree. Although Shanley is concerned with attaining a lock, Shanley fails to specifically disclose that the "nine offset values are 0 Hz; plus or minus 200 Hz; plus or minus 400 Hz; plus or minus 600 Hz; and plus or minus 800 Hz," as recited in claim 12 of the present invention. Therefore, as there is no mention or suggestion in Shanley of the nine offset values in claim 12, Shanley neither discloses nor suggests that the "nine offset values are 0 Hz; plus or minus 200 Hz; plus or minus 400 Hz; plus or minus 600 Hz; and plus or minus 800 Hz" as recited in claim 12 of the present invention.

Therefore as Shanley fails to show or suggest each feature in claim 12, Shanley does not anticipate the present claimed invention. As claim 13 is dependent on claim 12, claim 13 is also allowable for the same reasons as claim 12. Consequently, it is respectfully requested that the rejection of claims 12 and 13 under 35 U.S.C. 102(b) be withdrawn.

In view of the above remarks, Applicants respectfully submit that Shanley does not anticipate the present claimed invention as claimed in claims 1, 3-6, 8 and 10-13. Therefore, Applicants further respectfully submit that this rejection has been satisfied and should be withdrawn.

Rejection of claims 2 and 9 under 35 U.S.C. 103(a) over Shanley, II (U.S. Patent No. 4,617,587) in view of Wang (U.S. Patent No. 6,266,380)

Reversal of the rejection of claims 2 and 9 under 35 U.S.C. § 103(a) as being unpatentable over Shanley, II (U.S. Patent No. 4,617,587) in view of Wang (U.S. Patent No. 6,266,380) is respectfully requested because the rejection makes crucial errors in interpreting the cited references. The rejection erroneously states that claims 2 and 9 are made unpatentable by Shanley in view of Wang.

CLAIM 2

Claim 2 is dependent on claim 1 and is considered patentable for the reasons presented above with respect to claim 1. Additionally, Shanley, when taken alone or in combination with Wang, neither discloses nor suggests "calculating a preselected number of offset values for a desired symbol timing recovery range, said offset values being grouped substantially symmetrically about a central offset value" as recited in the present claimed invention. Moreover, Shanley and Wang neither disclose nor suggest "testing each of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value" as recited in the present claimed invention.

As described above with respect to claim 1, Shanley neither discloses nor suggests "calculating a preselected number of offset values for a desired symbol timing recovery range, said offset values being grouped substantially symmetrically about a central offset value" or "testing each of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value" as recited in claim 1 of the present invention. Additionally, even if the system of

Shanley was combined with the system of Wang, the combination would not make the present claimed invention unpatentable.

Wang describes a system for eliminating DC offset in a received HDTV signal. A receiver processes a VSB modulated signal containing terrestrial broadcast high definition television information. A pilot component includes an input analog-to-digital converter for producing a datastream which is oversampled at twice the received symbol rate. A segment sync detector uses an abbreviated correlation reference pattern to recover a twice symbol rate sampling clock for the digital converter. A DC offset associated with the pilot component is removed from the demodulated signal before it is applied to an NTSC interference detection network. However, similar to Shanley, Wang neither discloses nor suggests "**calculating a preselected number of offset values for a desired symbol timing recovery range**, said offset values being grouped substantially symmetrically about a central offset value" as recited in the present claimed invention. Wang is concerned with attenuating a DC component from a demodulated symbol datastream. This is unlike the present claimed invention which is concerned with establishing timing synchronism between a transmitter symbol clock and a local symbol clock in a receiver for receiving a signal transmitted as a sequence of symbols at a symbol frequency and subject to exhibiting a symbol frequency offset.

Additionally, since Wang is not concerned with and does not show the feature of calculating a preselected number of offset values for a desired symbol timing recover range, Wang (with Shanley) also cannot disclose or suggest "testing each of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value" as recited in claim 1 of present claimed invention. Wang describes a system for processing a received VSB signal containing high definition television information that includes a compensation network for processing an oversampled symbol datastream at the oversampling rate to remove a symbol DC offset component. Therefore, Wang is concerned with attenuating a DC component from a demodulated symbol datastream. This is unlike the present claimed invention which provides a preselected number of offset values for testing to achieve a desired symbol timing recovery lock quickly and accurately. Thus, Wang (and Shanley) neither discloses nor suggests "testing each

of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value" as recited in claim 1 of present claimed invention.

Applicants respectfully submit that there is no reason or motivation to combine Shanley with Wang. Shanley describes control loops for use in automatically establishing a desired condition of operation in an electrical apparatus, and a recovery system for use with the control loop to enable recovery from a failure mode in which a control voltage may be spuriously driven to a control voltage range extreme without establishing the desired operating condition. However, the television receiver in Shanley is an **analog** National Television System Committee (NTSC) receiver (see col. 2, lines 47-54) (or Phase Alternating Line (PAL) receiver). To the contrary, Wang describes a system for eliminating DC offset from a demodulated symbol datastream. Although Wang may deal with digital HDTV signals, as in the present claimed invention, Wang cannot be combined with Shanley. In the "Response to Arguments" section, it is argued that "it would have been obvious for one of ordinary skill at the time of the invention to combine the signal of Wang into the method and processor of Shanley. This would allow the received HDTV signal to be synchronized between the transmitter and receiver. This allows the recovery of the data to be performed correctly and with minimal errors." Applicants respectfully submit that such a combination of Wang and Shanley would yield an inoperable system. Specifically, the HDTV digital signal transmitted (as in Wang) cannot be received by the system of Shanley, which is only capable of dealing with analog NTSC signals. Shanley describes an "auxiliary apparatus" (col. 4, line 1) that adjusts "the free-running frequency of the oscillator" (col. 4, line 2) and keeps reducing "the difference relative to the burst subcarrier frequency" (col. 4, lines 3-4) until "a convergence to a condition where the phase locked loop locks up with static phase error substantially completely eliminated" (col. 4, lines 8-10) in an **analog television system**. Wang, on the other hand, provides an improved method of "processing an oversampled symbol datastream at the oversampling rate to remove a symbol DC offset component" (col. 1, lines 38-40) in a **digital HDTV system**. Shanley is not concerned with DC offset, as in Wang, because Shanley merely deals with analog television systems. Moreover, Wang is not concerned with converging to a condition where the free-running frequency of the oscillator is synchronized with the subcarrier frequency in an analog television system, as in Shanley, because Wang is

directed towards a digital television system. Therefore, the combination of Shanley and Wang would yield an inoperable system.

However, even if these two references were combined, as suggested by the Office Action, the combination of the system of Shanley with the system of Wang would not produce the present invention as claimed. Instead, the combined system would be an HDTV television receiver that synchronizes the free-running frequency of the oscillator with the subcarrier frequency to accurately avoid hue errors (or saturation errors) and eliminate DC offset in a VSB modulated signal. This is wholly unlike the present claimed invention. Specifically, the present claimed invention recites "**calculating a preselected number of offset values for a desired symbol timing recovery range**, said offset values being grouped substantially symmetrically about a central offset value" and "testing each of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value." The combined system of Shanley and Wang, similarly to the individual systems, neither discloses nor suggests such features. Consequently, it is respectfully submitted that the present invention as claimed is patentable over the cited reference when taken alone or in combination.

Therefore, Shanley and Wang neither disclose nor suggest the features claimed in claim 1 of the present invention. As claim 2 is dependent on claim 1, it is respectfully submitted that claim 2 is allowable over Shanley and Wang, when taken alone or in combination. Consequently, it is further respectfully requested that the rejection of claim 2 under 35 U.S.C. 103(a) be withdrawn.

CLAIM 9

Claim 9 is dependent on claim 8 and is considered patentable for the reasons presented above with respect to claim 8. Additionally, Shanley, when taken alone or in combination with Wang, neither discloses nor suggests "calculating a preselected number of offset values for a desired symbol timing recovery range, said offset values being grouped substantially symmetrically about a central offset value" as recited in the present claimed invention. Moreover, Shanley and Wang neither disclose nor suggest "testing each of said preselected offset

values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value" as recited in the present claimed invention.

As described above with respect to claim 8, Shanley neither discloses nor suggests "calculating a preselected number of offset values for a desired symbol timing recovery range, said offset values being grouped substantially symmetrically about a central offset value" or "testing each of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value" as recited in claim 8 of the present invention. Additionally, even if the system of Shanley was combined with the system of Wang, the combination would not make the present claimed invention unpatentable.

Wang describes a system for eliminating DC offset in a received HDTV signal. A receiver processes a VSB modulated signal containing terrestrial broadcast high definition television information. A pilot component includes an input analog-to-digital converter for producing a datastream which is oversampled at twice the received symbol rate. A segment sync detector uses an abbreviated correlation reference pattern to recover a twice symbol rate sampling clock for the digital converter. A DC offset associated with the pilot component is removed from the demodulated signal before it is applied to an NTSC interference detection network. However, similar to Shanley, Wang neither discloses nor suggests "**calculating a preselected number of offset values for a desired symbol timing recovery range**, said offset values being grouped substantially symmetrically about a central offset value" as recited in the present claimed invention. Wang is concerned with attenuating a DC component from a demodulated symbol datastream. This is unlike the present claimed invention which is concerned with establishing timing synchronism between a transmitter symbol clock and a local symbol clock in a receiver for receiving a signal transmitted as a sequence of symbols at a symbol frequency and subject to exhibiting a symbol frequency offset.

Additionally, since Wang is not concerned with and does not show the feature of calculating a preselected number of offset values for a desired symbol timing recover range,

Wang (with Shanley) also cannot disclose or suggest "testing each of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value" as recited in claim 8 of present claimed invention. Wang describes a system for processing a received VSB signal containing high definition television information that includes a compensation network for processing an oversampled symbol datastream at the oversampling rate to remove a symbol DC offset component. Therefore, Wang is concerned with attenuating a DC component from a demodulated symbol datastream. This is unlike the present claimed invention which provides a preselected number of offset values for testing to achieve a desired symbol timing recovery lock quickly and accurately. Thus, Wang (and Shanley) neither discloses nor suggests "testing each of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value" as recited in claim 8 of present claimed invention.

Applicants respectfully submit that there is no reason or motivation to combine Shanley with Wang. Shanley describes control loops for use in automatically establishing a desired condition of operation in an electrical apparatus, and a recovery system for use with the control loop to enable recovery from a failure mode in which a control voltage may be spuriously driven to a control voltage range extreme without establishing the desired operating condition. However, the television receiver in Shanley is an **analog** National Television System Committee (NTSC) receiver (*see* col. 2, lines 47-54) (or Phase Alternating Line (PAL) receiver). To the contrary, Wang describes a system for eliminating DC offset from a demodulated symbol datastream. Although Wang may deal with digital HDTV signals, as in the present claimed invention, Wang cannot be combined with Shanley. In the "Response to Arguments" section, it is argued that "it would have been obvious for one of ordinary skill at the time of the invention to combine the signal of Wang into the method and processor of Shanley. This would allow the received HDTV signal to be synchronized between the transmitter and receiver. This allows the recovery of the data to be performed correctly and with minimal errors." Applicants respectfully submit that such a combination of Wang and Shanley would yield an inoperable system. Specifically, the HDTV digital signal transmitted (as in Wang) cannot be received by the system of Shanley, which is only capable of dealing with analog NTSC signals. Shanley describes an

"auxiliary apparatus" (col. 4, line 1) that adjusts "the free-running frequency of the oscillator" (col. 4, line 2) and keeps reducing "the difference relative to the burst subcarrier frequency" (col. 4, lines 3-4) until "a convergence to a condition where the phase locked loop locks up with static phase error substantially completely eliminated" (col. 4, lines 8-10) in an **analog television system**. Wang, on the other hand, provides an improved method of "processing an oversampled symbol datastream at the oversampling rate to remove a symbol DC offset component" (col. 1, lines 38-40) in a **digital HDTV system**. Shanley is not concerned with DC offset, as in Wang, because Shanley merely deals with analog television systems. Moreover, Wang is not concerned with converging to a condition where the free-running frequency of the oscillator is synchronized with the subcarrier frequency in an analog television system, as in Shanley, because Wang is directed towards a digital television system. Therefore, the combination of Shanley and Wang would yield an inoperable system.

However, even if these two references were combined, as suggested by the Office Action, the combination of the system of Shanley with the system of Wang would not produce the present invention as claimed. Instead, the combined system would be an HDTV television receiver that synchronizes the free-running frequency of the oscillator with the subcarrier frequency to accurately avoid hue errors (or saturation errors) and eliminate DC offset in a VSB modulated signal. This is wholly unlike the present claimed invention. Specifically, the present claimed invention recites "**calculating a preselected number of offset values for a desired symbol timing recovery range**, said offset values being grouped substantially symmetrically about a central offset value" and "testing each of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value." The combined system of Shanley and Wang, similarly to the individual systems, neither discloses nor suggests such features. Consequently, it is respectfully submitted that the present invention as claimed is patentable over the cited reference when taken alone or in combination.

Therefore, Shanley and Wang neither disclose nor suggest the features claimed in claim 8 of the present invention. As claim 9 is dependent on claim 8, it is respectfully submitted that claim 9 is allowable over Shanley and Wang, when taken alone or in combination.

Consequently, it is further respectfully requested that the rejection of claim 9 under 35 U.S.C. 103(a) be withdrawn.

In view of the above remarks, it is respectfully submitted that there is no 35 USC 112 enabling disclosure in Shanley or Wang, when taken alone or in combination, which would make claims 2 and 9 of the present claimed invention unpatentable. Therefore, Applicants further respectfully submit that this rejection has been satisfied and should be withdrawn.

Rejection of claims 7 and 15 under 35 U.S.C. 103(a) over Shanley, II (U.S. Patent No. 4,617,587) in view of Guillemain et al. (U.S. Patent No. 6,175,600)

Reversal of the rejection of claims 7 and 15 under 35 U.S.C. § 103(a) as being unpatentable over Shanley, II (U.S. Patent No. 4,617,587) in view of Guillemain (U.S. Patent No. 6,175,600) is respectfully requested because the rejection makes crucial errors in interpreting the cited references. The rejection erroneously states that claims 7 and 15 are made unpatentable by Shanley in view of Guillemain.

CLAIM 7

Claim 7 is dependent on claims 1 and 6 and is considered patentable for the reasons presented above with respect to claims 1 and 6. Additionally, Shanley with Guillemain, neither discloses nor suggests "calculating a preselected number of offset values for a desired symbol timing recovery range, said offset values being grouped substantially symmetrically about a central offset value" as recited in the present claimed invention. Moreover, Shanley, with Guillemain, neither discloses nor suggests "testing each of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value" as recited in the present claimed invention.

As described above with respect to claim 1, Shanley neither discloses nor suggests "calculating a preselected number of offset values for a desired symbol timing recovery range, said offset values being grouped substantially symmetrically about a central offset value" or

"testing each of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value" as recited in claim 1 of the present invention. Additionally, even if the system of Shanley was combined with the system of Guillemain, the combination would not make the present claimed invention unpatentable.

Guillemain describes a system for detecting the presence of a carrier wave in a digital signal that is available at a given frequency. The system delivers at least two baseband samples of the digital signal at each symbol time. A timing estimator responds to the baseband samples to provide an error signal corresponding to a phase error between the clock frequency that is to be recovered and a local clock frequency. A detection signal is generated when a level representative of the variance of the error signal reaches a threshold value. However, similar to Shanley, Guillemain neither discloses nor suggests "**calculating a preselected number of offset values for a desired symbol timing recovery range**, said offset values being grouped substantially symmetrically about a central offset value" as recited in the present claimed invention. Guillemain is concerned with detecting the presence or the absence of a signal carrier wave that is present at a given clock frequency. This is unlike the present claimed invention which is concerned with establishing timing synchronism between a transmitter symbol clock and a local symbol clock in a receiver for receiving a signal transmitted as a sequence of symbols at a symbol frequency and subject to exhibiting a symbol frequency offset.

Additionally, since Guillemain is not concerned with calculating a preselected number of offset values for a desired symbol timing recover range, Guillemain also cannot disclose or suggest "testing each of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value" as recited in claim 1 of present claimed invention. Guillemain describes a timing estimator responsive to the baseband samples for delivering an error signal corresponding to the phase error between the clock frequency that is to be recovered and a local frequency. A detector generates a detection signal indicating that a carrier wave has been detected whenever a level representative of the variance of the error signal reaches a threshold value. Therefore, Guillemain is concerned with detecting the presence of a carrier wave in a digital signal that is

available at a given frequency. This is wholly unlike the present claimed invention which provides a preselected number of offset values for testing to achieve a desired symbol timing recovery lock quickly and accurately. Thus, Guillemain neither discloses nor suggests "testing each of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value" as recited in claim 1 of present claimed invention.

Applicants respectfully submit that there is no reason or motivation to combine Shanley with Guillemain. Shanley describes control loops for use in automatically establishing a desired condition of operation in an electrical apparatus, and a recovery system for use with the control loop to enable recovery from a failure mode in which a control voltage may be spuriously driven to a control voltage range extreme without establishing the desired operating condition. Guillemain describes a system detecting the presence of a carrier wave in a digital signal that is available at a given frequency. These references are responsive to different problems and thus, it is respectfully submitted that the combination of these references to produce the present invention would not be obvious. Shanley describes an "auxiliary apparatus" (col. 4, line 1) that adjusts "the free-running frequency of the oscillator" (col. 4, line 2) and keeps reducing "the difference relative to the burst subcarrier frequency" (col. 4, lines 3-4) until "a convergence to a condition where the phase locked loop locks up with static phase error substantially completely eliminated" (col. 4, lines 8-10). Guillemain, on the other hand, provides an improved method of detecting the presence of a signal carrier wave that combines "speed, reliability, operation at a poor ED/No ratio (close to 2 dB), and is relatively insensitive to drift in the frequency of the carrier wave" (col. 2, lines 23-29).

However, even if the systems of Shanley and Guillemain were combined, the combined system would not produce the present invention as claimed. Instead, the combined system would yield a system that synchronizes the free-running frequency of the oscillator with the subcarrier frequency to accurately avoid hue errors (or saturation errors) in a television system and detects the presence or absence of a signal carrier wave at a given frequency. This is wholly unlike the present claimed invention. Specifically, the present claimed invention recites "**calculating a preselected number of offset values for a desired symbol timing recovery range**, said offset

values being grouped substantially symmetrically about a central offset value." The combined system of Shanley and Guillemain, similarly to the individual systems, neither discloses nor suggests such features. Consequently, it is respectfully submitted that the present invention as claimed is patentable over the cited reference when taken alone or in combination.

Therefore, Shanley and Guillemain neither disclose nor suggest the features claimed in claim 8 of the present invention. As claim 7 is dependent on claim 8, it is respectfully submitted that claim 7 is allowable over Shanley and Guillemain, when taken alone or in combination. Consequently, it is further respectfully requested that the rejection of claim 7 under 35 U.S.C. 103(a) be withdrawn.

CLAIM 15

Claim 15 is dependent on claims 8 and 13 and is considered patentable for the reasons presented above with respect to claims 8 and 13. Additionally, Shanley with Guillemain, neither discloses nor suggests "calculating a preselected number of offset values for a desired symbol timing recovery range, said offset values being grouped substantially symmetrically about a central offset value" as recited in the present claimed invention. Moreover, Shanley, with Guillemain, neither discloses nor suggests "testing each of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value" as recited in the present claimed invention.

As described above with respect to claim 8, Shanley neither discloses nor suggests "calculating a preselected number of offset values for a desired symbol timing recovery range, said offset values being grouped substantially symmetrically about a central offset value" or "testing each of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value" as recited in claim 8 of the present invention. Additionally, even if the system of Shanley was combined with the system of Guillemain, the combination would not make the present claimed invention unpatentable.

Guillemain describes a system for detecting the presence of a carrier wave in a digital signal that is available at a given frequency. The system delivers at least two baseband samples of the digital signal at each symbol time. A timing estimator responds to the baseband samples to provide an error signal corresponding to a phase error between the clock frequency that is to be recovered and a local clock frequency. A detection signal is generated when a level representative of the variance of the error signal reaches a threshold value. However, similar to Shanley, Guillemain neither discloses nor suggests "**calculating a preselected number of offset values for a desired symbol timing recovery range**, said offset values being grouped substantially symmetrically about a central offset value" as recited in the present claimed invention. Guillemain is concerned with detecting the presence or the absence of a signal carrier wave that is present at a given clock frequency. This is unlike the present claimed invention which is concerned with establishing timing synchronism between a transmitter symbol clock and a local symbol clock in a receiver for receiving a signal transmitted as a sequence of symbols at a symbol frequency and subject to exhibiting a symbol frequency offset.

Additionally, since Guillemain is not concerned with and does not show the feature of calculating a preselected number of offset values for a desired symbol timing recover range, Guillemain also cannot disclose or suggest "testing each of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value" as recited in claim 8 of present claimed invention. Guillemain describes a timing estimator responsive to the baseband samples for delivering an error signal corresponding to the phase error between the clock frequency that is to be recovered and a local frequency. A detector generates a detection signal indicating that a carrier wave has been detected whenever a level representative of the variance of the error signal reaches a threshold value. Therefore, Guillemain is concerned with detecting the presence of a carrier wave in a digital signal that is available at a given frequency. This is wholly unlike the present claimed invention which provides a preselected number of offset values for testing to achieve a desired symbol timing recovery lock quickly and accurately. Thus, Guillemain neither discloses nor suggests "testing each of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value" as recited in claim 8 of present claimed invention.

Applicants respectfully submit that there is no reason or motivation to combine Shanley with Guillemain. Shanley describes control loops for use in automatically establishing a desired condition of operation in an electrical apparatus, and a recovery system for use with the control loop to enable recovery from a failure mode in which a control voltage may be spuriously driven to a control voltage range extreme without establishing the desired operating condition. Guillemain describes a system detecting the presence of a carrier wave in a digital signal that is available at a given frequency. These references are responsive to different problems and thus, it is respectfully submitted that the combination of these references to produce the present invention would not be obvious. Shanley describes an "auxiliary apparatus" (col. 4, line 1) that adjusts "the free-running frequency of the oscillator" (col. 4, line 2) and keeps reducing "the difference relative to the burst subcarrier frequency" (col. 4, lines 3-4) until "a convergence to a condition where the phase locked loop locks up with static phase error substantially completely eliminated" (col. 4, lines 8-10). Guillemain, on the other hand, provides an improved method of detecting the presence of a signal carrier wave that combines "speed, reliability, operation at a poor ED/No ratio (close to 2 dB), and is relatively insensitive to drift in the frequency of the carrier wave" (col. 2, lines 23-29).

However, even if the systems of Shanley and Guillemain were combined, the combined system would not produce the present invention as claimed. Instead, the combined system would yield a system that synchronizes the free-running frequency of the oscillator with the subcarrier frequency to accurately avoid hue errors (or saturation errors) in a television system and detects the presence or absence of a signal carrier wave at a given frequency. This is wholly unlike the present claimed invention. Specifically, the present claimed invention recites "**calculating a preselected number of offset values for a desired symbol timing recovery range**, said offset values being grouped substantially symmetrically about a central offset value." The combined system of Shanley and Guillemain, similarly to the individual systems, neither discloses nor suggests such features. Consequently, it is respectfully submitted that the present invention as claimed is patentable over the cited reference when taken alone or in combination.

Therefore, Shanley and Guillemain neither disclose nor suggest the features claimed in

claim 8 of the present invention. As claim 15 is dependent on claim 8, it is respectfully submitted that claim 15 is allowable over Shanley and Guillemain, when taken alone or in combination. Consequently, it is further respectfully requested that the rejection of claim 7 under 35 U.S.C. 103(a) be withdrawn.

In view of the above remarks, it is respectfully submitted that there is no 35 USC 112 enabling disclosure in Shanley or Guillemain, when taken alone or in combination, which would make claims 7 and 15 of the present claimed invention unpatentable. Therefore, Applicants further respectfully submit that this rejection has been satisfied and should be withdrawn.

CLAIM 14

Claim 14 is dependent on claims 8 and 13 and is allowable for the same reasons presented above with respect to claims 8 and 13. The Office Action does not reject claim 14 under the 102(b) or either of the 103(a) rejections. However, Applicants respectfully submit that claim 14 is allowable over Shanley, Wang and Guillemain, when taken alone or in any combination. Consequently, claim 14 is allowable over Shanley, Wang and Guillemain.

VIII CONCLUSION

Shanley, Wang and Guillemain, when taken alone or in any combination, do not disclose or suggest "calculating a preselected number of offset values for a desired symbol timing recovery range, said offset values being grouped substantially symmetrically about a central offset value; testing each of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value" as recited in claim 1 of the present claimed invention. As claims 1 and 8 include similar subject matter, these claims are all allowable over Shanley, Wang and Guillemain, when taken alone or in any combination. As claims 2-7 and 9-15 are dependent on claims 1 and 8, respectively, these claims are also allowable over Shanley, Wang and Guillemain.

Accordingly it is respectfully submitted that the rejection of claims 1-15 should be reversed.

Respectfully submitted,
Weixiao Liu et al.

By: _____
Jack Schwartz
Reg. No. 34,721
Tel. No. (609) 734-6866

Thomson Licensing, LLC
Patent Operations
PO Box 5312
Princeton, NJ 08543-5312
February 27, 2008

APPENDIX I - APPEALED CLAIMS

1. (Original) A method for establishing timing synchronism between a transmitter symbol clock and a local symbol clock in a receiver for receiving a signal transmitted as a sequence of symbols at a symbol frequency and subject to exhibiting a symbol frequency offset, said method comprising the steps of:

calculating a preselected number of offset values for a desired symbol timing recovery range, said offset values being grouped substantially symmetrically about a central offset value;

testing each of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value.

2. (Original) A method of claim 1 wherein the received signal carries a high definition television (HDTV) signal transmitted as a modulated vestigial sideband (VSB) signal formatted as a one-dimensional data constellation of symbols representing digital image data.

3. (Original) A method as claimed in claim 1 wherein said desired symbol timing recovery range is plus or minus 1 kHz.

4. (Original) A method as claimed in claim 3 wherein said preselected number of offset values is nine.

5. (Original) A method as claimed in claim 4 wherein said nine offset values are 0 Hz; plus or minus 200 Hz; plus or minus 400 Hz; plus or minus 600 Hz; and plus or minus 800 Hz.

6. (Original) A method as claimed in claim 1 further comprising steps of repeating the testing step for each of a plurality of symbol timing recovery algorithms.

7. (Original) A method as claimed in claim 6 wherein said plurality of symbol timing recovery algorithms comprises the Mueller and Muller algorithm and the Gardner algorithm.

8. (Original) A processor for establishing timing synchronism between a transmitter symbol clock and a local receiver symbol clock in a receiver for receiving a signal comprising a sequence of symbols at a symbol frequency and subject to exhibiting symbol frequency offset comprising:

means for calculating a preselected number of offset values for a desired symbol timing recovery range, said offset values being grouped substantially symmetrically about a central offset value;

means for testing each of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value.

9. (Original) A processor as claimed in claim 8 wherein the received signal comprises a high definition television (HDTV) signal transmitted as a one-dimensional data constellation of symbols representing digital image data.

10. (Original) A processor as claimed in claim 8 wherein said desired symbol timing recovery range is plus or minus 1 KHz.

11. (Original) A processor as claimed in claim 10 wherein said preselected number of offset values is nine.

12. (Original) A processor as claimed in claim 11 wherein said nine offset values are 0 Hz; plus or minus 200 Hz; plus or minus 400 Hz; plus or minus 600 Hz; and plus or minus 800 Hz.

13. (Original) A processor as claimed in claim 12 further comprising:

means for using a plurality of symbol timing detection algorithms for said testing; and

means for switching between said algorithms as desired to maximize the possibility of STR lock.

14. (Original) A processor as claimed in claim 13 wherein the switching means comprises means for selecting one of the plurality of detection algorithms before testing each of said preselected offset values.

15. (Original) A processor as claimed in claim 13 wherein said plurality of timing detection algorithms comprise the Mueller and Muller algorithm and the Gardner algorithm.

APPENDIX II - EVIDENCE

Applicant does not rely on any additional evidence other than the arguments submitted hereinabove.

APPENDIX III - RELATED PROCEEDINGS

Applicant respectfully submits that there are no proceedings related to this appeal in which any decisions were rendered.

APPENDIX IV - TABLE OF CASES

APPENDIX V - LIST OF REFERENCES

U.S. Pat. No.	Issued Date	102(e) Date	Inventors
4,617,587	October 14, 1986		Shanley, II
6,266,380	July 24, 2001		Wang
6,175,600	January 16, 2001		Guillemain et al.

TABLE OF CONTENTS